REMARKS

Claims 1-15 are pending. Claims 1-15 have been rejected as anticipated by U.S. Patent 6,510,530 (hereinafter referred to as "Wu"). Applicants traverse the rejections.

Wu discloses a compact static RAM (CsRAM) chip [col. 1, lines 13-29] with a Built-in Self-Test (BIST) controller [col.2, lines 39-41]. Wu further discloses a BIST approach to achieve at-speed testing for compact sRAMs 10, having a working speed at least "k" times faster than the system clock generator 12 [col. 11, lines 56-59]. Wu neither discloses nor suggests a programmable logic device (PLD) such as, for example, a field programmable gate array (FPGA).

Claim 1 includes among other features, selecting by a selection device between source signals to drive a shared programmable interconnect portion located on the programmable logic device. As supported by the "description of related art" in the specification, the programmable interconnect can be programmed to different routing configurations by a user. The shared interconnect portion between 15 and 17/19 of FIG. 1A in Wu as cited by the Examiner is not a programmable interconnect portion located on a programmable logic device. The shared interconnect portion between 15 and 17/19 is fixed (i.e., not programmable) and on a memory circuit , not a PLD. Thus amended claim 1 should be allowable.

Claims 2-9 being dependent upon claim 1 should be allowable for at least the reasons claim 1 is allowable.

Claim 10 includes among other features, selecting by a selection device between source signals to route signals onto a shared programmable interconnect on the programmable logic device and routing signals from the shared programmable interconnect to the capture devices through a first programmable interconnect point. Programmable interconnect points as supported by paragraphs [0030]-[0031] and FIG. 4A of the specification are interconnect points that can be programmed to be open or closed to give different routing paths. In addition to the reasons given for claim 1 above being allowable, Applicants traverse the Examiner's assertion that a programmable interconnect point is "inherent". The Applicant requests a reference to support the Examiner's assertion of a programmable interconnect point being inherent

in a CsRAM, otherwise the Applicants assert the Examiner is not only being conclusory, but has no basis for his/her conclusion. For these reasons and the reasons given in claim 1, claim 10 should be allowable.

Claims 11-12 being dependent upon claim 1 should be allowable for at least the reasons claim 10 is allowable.

Claim 13 includes among other features, a multiplexer which chooses between source signals to drive a shared programmable interconnect on the programmable logic device. The shared interconnect portion between 15 and 17/19 of FIG. 1A in Wu as cited by the Examiner is not a programmable interconnect portion located on a programmable logic device. The shared interconnect portion between 15 and 17/19 is fixed (i.e., not programmable) and on a memory circuit, not a PLD. Thus amended claim 13 should be allowable.

Claims 14-15 being dependent upon claim 13 should be allowable for at least the reasons claim 13 is allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

Kim Kanzaki, Ph.D.
Attorney for Applicant
Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 20, 2005.

Pat Tompkins
Name

Pat Tompkins
Signature